CLAIMS

What is claimed is:

1. A circuit for electrostatic discharge (ESD) protection, comprising:

   a. a low capacitance ESD protection circuit coupled to a pad and a ground;

   b. a first resistive device, comprising a first connection coupled to the pad and a second connection; and

   c. a second device coupled to the second connection of the first resistive device and to the ground.

2. The circuit of claim 1, wherein the pad is at least one of (a) an input/output power pad or (b) an input/output signal pad.

3. The circuit of claim 1, wherein the first resistive device comprises a low impedance resistor.

4. The circuit of claim 3, wherein the low impedance resistor comprises an impedance of between about 1 ohm to 100 ohms.

5. The circuit of claim 1, wherein the second device comprises an NMOS transistor.

6. The circuit of claim 5, wherein the source of the NMOS transistor and the gate of the NMOS transistor are coupled to a common junction.

7. The circuit of the claim 6, wherein the common junction is the ground.

8. An integrated circuit, comprising:

   a. a pad;

   b. a buffer circuit, operatively coupled to a voltage terminal and to a ground;

   c. an internal circuit, operatively coupled to the voltage terminal and to the ground;

d. a low capacitance electrostatic discharge (ESD) protection circuit coupled to the pad and the ground;

e. a first resistive device, comprising a first connection coupled to the pad and a second connection coupled to the buffer circuit; and

f. a second device coupled to the second connection of the first resistive device and to the ground.

9. The integrated circuit of claim 8, wherein the buffer circuit comprises an inverter.

10. The integrated circuit of claim 8, wherein the first resistive device comprises a low impedance resistor.

11. The circuit of claim 10, wherein the low impedance resistor comprises an impedance of between about 1 ohm to 100 ohms.

12. The circuit of claim 8, wherein the second device comprises an NMOS transistor.

13. The circuit of claim 12, wherein the source of the NMOS transistor and the gate of the NMOS transistor are coupled to a common junction.

14. The circuit of the claim 13, wherein the common junction is ground.

15. The circuit of claim 8 wherein:

a. the voltage terminal is a V_{SS} voltage terminal; and

b. the first resistive device and the second device effect a current path between the V_{SS} terminal and the pad.

16. The circuit of claim 11, wherein the NMOS has a width from about 10 μm to about 30 μm and has a length from about 0.15 μm to about 0.25 μm.

17. A method of protecting an internal circuit from electrostatic discharge (ESD), comprising:

a. coupling a functional circuit to an ESD protection circuit;

b. coupling the ESD protection circuit to a pad;

c. operatively coupling an additional circuit intermediate the ESD protection circuit and the functional circuit; and

d. using the additional circuit to effect a voltage drop between the pad and the functional circuit to protect thin oxide layers of at least a portion of the functional circuit from damage when an ESD pulse is present at the pad.

18. The method of claim 17, wherein using the additional circuit further comprises a device adapted to increase resistance between the pad and the functional circuit.

19. The method of claim 18, wherein the resistance is from about 1 ohm to about 100 ohms.

20. The method of claim 17 further comprising discharging the ESD pulse to a V_{SS} terminal when the ESD pulse is coupled to the pad.

21. The method of claim 17 further comprising disabling a current path formed by the coupling of the functional circuit to the ESD protection circuit when no ESD pulse is coupled to the pad.

22. The method of claim 21, wherein discharging the ESD pulse further comprises punching through a MOS transistor.